An Ultra-broadband, High Gain CMOS Distributed Amplifier Based on a New Gain Cell in 0.13 µm Technology

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Abstract—In this paper a high gain and ultra-broadband CMOS distributed amplifier (CMOS-DA) utilizing standard 0.13 µm CMOS technology is presented. This design is based on a new gain cell that makes an ultra-broadband DA by considering the gain, noise figure (NF), input and output return losses concurrently. The new gain cell is the improved version of active cascode that enhances the output impedance as a result the gain substantially over conventional active cascode. The DA achieved a flat and high power gain (S21) of 17.5 ± 0.5 dB with a 3-dB bandwidth of 21 GHz and a power dissipation (Pdc) of 63.3 mW. It has an average NF of as low as 3.58 dB, while its input and output matches of less than -10 dB in the entire interest band.

Keywords—active cascode amplifier; CMOS distributed amplifier; ultra-broadband; high-gain; low noise

I. INTRODUCTION

Recent performance enhancements derived thanks to modern CMOS technology’s aggressive scaling. They including higher level of integration, lower cost, and intrinsic high-speed transistors that have become the most promising technology to realize high-speed broadband communication circuits [1, 2]. Broadband amplifiers are the critical building blocks in various fields such as high-speed links, high-resolution radar, imaging systems, electronic warfare, and broadband commercial or military radio systems [3]. Distributed amplifiers (DAs) by taking benefit of several parallel signal paths also the distribution of the parasitic capacitors of active devices in a low-pass LC section can satisfy a proper gain-bandwidth trade-off [4, 5].

Reference [5] introduces a 0.18 µm CMOS-DA utilizing a cascaded gain cell that shaped through an inductively parallel-peaking cascode stage with a low Q-RC load and an inductively series-peaking common-source (CS) stage. The DA achieved excellent flat and high gain of 20.47 ± 0.72 dB and an average noise figure (NF) of 3.3 dB at high gain (HG) mode. At low gain (LG) mode it obtained the power gain of 11.03 ± 0.98 dB and an average NF of 4.25 dB. Nevertheless, the corresponding 3-dB bandwidth only covered the ultra-wideband (UWB) ranges of frequencies. The design of [3] has a power gain of 20.5 dB, and a 3-dB bandwidth of 35 GHz but, the desire gain-bandwidth performance is achieved at the cost of huge chip size and high power dissipation that are not satisfactory.

Finally the design of [4] reports a 0.18 µm CMOS-DA that formed by two enhanced CMOS inverters. Also the DA utilizes multiple noise suppression techniques. However, it suffers a restricted 3-dB bandwidth of 1.2 ~ 8.6 GHz in LG mode and 1.5 ~ 8.2 GHz in HG mode that doesn’t support even the entire UWB of frequencies. To demonstrate that the flat and high power gain and ultra-broad bandwidth can be achieved concurrently in a CMOS-DA we present a CMOS-DA based on a new gain cell.

II. CIRCUIT DESIGN

High gain DAs are designed into two classes to date. DAs based on cascaded gain cell that increase the amplifier’s gain while operating in low voltage and low power conditions. But this group suffer from poor closed loop stability and lack of an ultra-broad band response, due to the incurrence of multiple poles by cascaded amplifiers [6, 7].

The other class introduces two-dimensional DAs, such as cascaded multi-stage distributed amplifier (CMSDA) [8], DA with cascaded gain stages [9], combination of the conventional DA (CDA) and the cascaded single stage DA (CSSDA) [3], and matrix DAs [10]. This class apply the multiplicative gain mechanism, to meet the high gain performance. Although this group has higher gain-bandwidth performance than other, but their huge chip size and power dissipation aren’t desire. Fig. 1 shows the schematic of the proposed CMOS-DA.
Unlike exiting high gain DAs that mentioned above the new CMOS-DA presents a high gain and ultra-broadband response at the same time. It alleviates the defect of cascaded gain cells in the point of restricted bandwidth and overcomes to shortcomings of two dimensional DAs including high power dissipation and big chip area.

To meet the desire specifications including a high gain and ultra-broadband response concurrently, Advanced Active Cascode (AAC) is proposed for gain cell. The simple active cascode increases the output impedance to obtain the higher gain. This advantage obtains without, any limiting in the power-supply voltage and signal-swing requirements that are unavoidable in conventional cascode topologies. As can be seen in Fig. 2 (a), the active cascode circuit utilizes an amplifier in a negative feedback loop to control the voltage from the gate of $M_2$ to ground. The idea is drive the gate of $M_2$ by an amplifier that forces the voltage produced across drain of $M_1$ to be equal to gate voltage of $M_2$.

In this way the current-voltage negative feedback is realized that increases the output impedance significantly without staking more cascode devices on top of $M_2$ [11]. AAC is an effort towards the further increasing output impedance as a result gain to that of the conventional active cascode. AAC by replacing the CS cell with active cascode amplifier in negative feedback loop as shown in Fig. 2(c) boosted the output impedance significantly over conventional active cascode, hence the higher gain performance is achieved.

Fig. 1. The proposed CMOS-DA

Fig. 2. (a) Active cascode amplifier (b) Active cascode amplifier with CS cell as $a_1 (c)$ Advanced Active Cascode amplifier (AAC)
It obtained in the fact that, the voltage gain of active cascode as the amplifier that realizes the negative feedback loop is significantly higher than CS cell. One can prove the small-signal voltage gain of conventional active cascode and AAC are given according to (1) to (4):

\[
A_v = g_{m1}R_{out} \quad \& \quad R_{out} = (a_1 + 1) g_{m2} r_{o1} r_{o2} \quad (1)
\]

\[
A_v = g_{m1} (a_1 + 1) g_{m2} r_{o1} r_{o2}. \quad (2)
\]

In the primary case a_1 amplifier is a CS cell as shown in Fig.2 (b), which in this case the small-signal voltage gain can be expressed as follows:

\[
A_v = g_{m1} g_{m2} g_{m3} r_{o1} r_{o2} r_{o3}. \quad (3)
\]

While in the case of AAC gain cell we have:

\[
A_v = g_{m1} (g_{m3} g_{m4} g_{m5} r_{o1} r_{o2} r_{o3} r_{o5}) g_{m2} r_{o1} r_{o2}. \quad (4)
\]

Where \( g_{mi} \) and \( r_{oi} \) are the transconductance and the output resistors of the \( M_i \) for \( i = 1, 2, 3 \) respectively. Comparing the small-signal gain of AAC to that of the simple active cascode, shows the gain of simple active cascode is similar to triple customary cascode while the gain of AAC is similar to the gain of quintuplet cascode amplifier.

### III. Simulation & Results

Simulation results were generated via Advanced Design System (ADS) software in 0.13 µm CMOS technology. The number of stages are adopted in optimum mode and obtained three stages. The simulation results are illustrated in Figs 3 ~ 6. The power gain and reverse isolation are plotted in Fig. 3 that the average power gain is about 17.5 dB with a 3-dB frequency band of DC up to 21 GHz. The reverse isolation is better than -25 dB. The simulated input and output return losses are provided in Fig. 4 which both are below than -10 dB. Figs 5 & 6 display the simulated average NF and stability-factor (k). The average NF achieved value of as low as 3.58 dB also the DA unconditionally stabled over the frequencies of interest. The CMOS-DA dissipates 63.3 mW.

The performances of the new CMOS-DA with some other recently published works in 0.18 µm and 0.13 µm CMOS technologies are compared in table I. The simulated results presented good performances in terms of bandwidth and gain at the same time while the good impedance matching and NF obtained.
A high gain and ultra-broadband CMOS-DA has been reported. It adopted a new gain cell that remove the shortcomings of either cascade gain cells including restricted bandwidth and cascade gain cells cosigning limited signal swings. A proposed CMOS-DA topology can give a significant gain of 17.5 dB and an ultra-broad bandwidth of DC up to 21 GHz. The simulated results of the gain, input and output return losses, isolation, and NF illustrated the capability of utilizing this device for ultra-broadband applications.

IV. CONCLUSION

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![Simulated stability-factor graph](image)

**Fig. 6. Simulated stability-factor (k)**

<table>
<thead>
<tr>
<th>references</th>
<th>process</th>
<th>Freq (GHz)</th>
<th>Gain (dB)</th>
<th>Average NF (dB)</th>
<th>$S_{11}$ (dB)</th>
<th>$S_{22}$ (dB)</th>
<th>$p_{in}$ (mw)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[4] 2011* (HG mode)</td>
<td>0.18μm CMOS</td>
<td>1.5 - 8.2</td>
<td>17.1 ± 1.5</td>
<td>3.52</td>
<td>&lt; -11</td>
<td>&lt; -10.1</td>
<td>46.85</td>
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<tr>
<td>[4] 2011* (LG mode)</td>
<td>0.13μm CMOS</td>
<td>1.2 - 8.6</td>
<td>11.4 ± 1.4</td>
<td>3.74</td>
<td>&lt; -9.4</td>
<td>&lt; -10.4</td>
<td>9.85</td>
</tr>
<tr>
<td>[5] 2011* (HG mode)</td>
<td>0.13μm CMOS</td>
<td>0.4 - 10.5</td>
<td>20.47 ± 0.72</td>
<td>3.29</td>
<td>&lt; -10</td>
<td>&lt; -10</td>
<td>37.8</td>
</tr>
<tr>
<td>[5] 2011* (LG mode)</td>
<td>0.13μm CMOS</td>
<td>0.7 - 10.9</td>
<td>11.03 ± 0.98</td>
<td>4.25</td>
<td>&lt; -10.3</td>
<td>&lt; -10.9</td>
<td>6.86</td>
</tr>
<tr>
<td>[6] 2013* (HG mode)</td>
<td>0.13μm CMOS</td>
<td>0 - 11</td>
<td>20.5 ± 0.5</td>
<td>7.5</td>
<td>&lt; -11</td>
<td>&lt; -18</td>
<td>9.36</td>
</tr>
<tr>
<td>[6] 2013* (LG mode)</td>
<td>0.13μm CMOS</td>
<td>0 - 12</td>
<td>15.5 ± 0.25</td>
<td>7</td>
<td>&lt; -11.5</td>
<td>&lt; -16.5</td>
<td>3.6</td>
</tr>
<tr>
<td>[3] 2013*</td>
<td>0.18μm CMOS</td>
<td>35</td>
<td>20.5</td>
<td>7.4</td>
<td>&lt; -12</td>
<td>&lt; -14</td>
<td>250</td>
</tr>
<tr>
<td>This work</td>
<td>0.13μm CMOS</td>
<td>DC - 21</td>
<td>17.3 ± 0.5</td>
<td>3.58</td>
<td>&lt; -10</td>
<td>&lt; -11</td>
<td>63.3</td>
</tr>
</tbody>
</table>

**TABLE I. PREVIOUSLY PUBLISHED CMOS-DAS AGAINST THE PROPOSED CMOS-DA**

- a: Based on measurement results
- b: Based on simulated results

REFERENCES